amendment. The attached page(s) is captioned "**Version With Markings To Show Changes Made.**"

For purposes of example and without limitation, certain example embodiments of this invention relate to a method of making a semiconductor device. Referring to Figs. 1A-1E of the instant application, for example, the method includes forming an interlayer insulating film 2 and a barrier film 3 on a semiconductor substrate 1. A contact hole 2a is then formed *at the same time* and of the same size in *both* the barrier film 3 and the interlayer insulating film 2 (e.g., see Fig. 1A). Then, a plug (4 and/or 5) is formed within the contact hole 2a (see Fig. 1A), and an insulation film 6 is formed on the plug 4/5 and the barrier film 3. A hole 6a is then formed in the insulation film 6 leading to the plug so that an upper surface of the plug as well as *part of the barrier film 3 are exposed* (e.g., see Fig. 1B). A first conductive film 7 is then formed on the insulation film 6 and *on and over the exposed part of the barrier film* 3 in hole 6a so that the hole 6a in the insulation film 6 is filled with the first conductive film 7 (e.g., see Fig. 1B). The first conductive film 7 is then etched (e.g., via CMP) to form a lower electrode 8 within the hole in the insulation film 6 (see Fig. 1C). The *insulation film 6 is then etched until the barrier film 3 is exposed* (see Fig. 1D), so as to leave the lower electrode 8 in a protuberant manner. A dielectric film (e.g., ferroelectric) 9 is then formed to cover the protuberant lower electrode 8 and at least part of the barrier film 3, and a second conductive film 10 is formed to cover at least part of the dielectric film 9. Another example embodiment is illustrated in Fig. 2.

Claim 1 is intended to read on at least the Fig. 1 embodiment, while claim 4 is intended to read on at least the Fig. 2 embodiment.

Claim 1 stands rejected under 35 U.S.C. Section 102(e) as being allegedly anticipated by Hieda. This Section 102(e) rejection is respectfully traversed for at least the following reasons.

Claim 1 requires "making a contact hole in the barrier film and the interlayer insulating film *at the same time* and forming a plug within the contact hole; forming an insulation film on the plug and the barrier film and then forming a hole in the insulation film leading to the plug such that an upper surface of the plug and *part of the barrier film are exposed*; forming a first conductive film on the insulation film and *on and over an exposed part of the barrier film* in the hole such that the hole in the insulation film is filled with the first conductive film, and then etching the first conductive film by a chemical mechanical polishing method to thereby form a lower electrode within the hole in the insulation film; etching the insulation film until the barrier film is exposed, so as to leave the lower electrode in a protuberant manner . . . . patterning the dielectric film and the second conductive film simultaneously to thereby form a capacitor dielectric film and an upper electrode." For example, referring to Fig. 1, a contact hole 2a is formed in the barrier film 3 and the interlayer insulating film 2 at the same time, with plug 4/5 thereafter being formed within the contact hole 2a (see Fig. 1A). Then, an insulation film 6 is formed on the plug 4/5 and the barrier film 3, and hole 6a is formed in the insulation film 6 so that an upper surface of the plug and part of the barrier film 3 are exposed. Thereafter, a first conductive film 7 is formed on the insulation film 6 and on and over an

exposed part of the barrier film 3 in the hole 6a such that the hole 6a in the insulation film is filled with the first conductive film 7 (see Fig. 1B). Then, the first conductive film 7 is etched by a chemical mechanical polishing method to form a lower electrode 8 within the hole 6a in the insulation film 6 (see Fig. 1C). Thereafter, the insulation film 6 is etched until the barrier film 3 is exposed, so as to leave the lower electrode 8 in a protuberant manner (see Fig. 1D). The cited art fails to disclose or suggest the aforesaid underlined aspects of claim 1.

Hieda in Figs. 19-20 illustrates formation of an alleged silicon nitride barrier film 21 and an oxide insulator 22 over an interlayer insulator 14, 15. A small contact hole is formed in the interlayer insulator 14, 15 and filled with a conductive plug, while at a *later point in time* a much larger hole is defined in the alleged barrier nitride film 21and oxide film 22 to be filled with electrode 24.

Claim 1 requires "making a contact hole in the barrier film and the interlayer insulating film *at the same time*." Thus, assuming that Hieda's layer 14 is an "interlayer insulator" as alleged in the Office Action, the nitride film 21 cannot possibly be the claimed "barrier film." This is because the holes in layers 14 and 21 are formed at very different points in time in Hieda (i.e., the hole in layer 21 is formed well after the hole in layer 14). Yet another reason why Hieda's nitride film 21 cannot possibly be the claimed "barrier film" is that claim 1 requires "forming a first conductive film on the insulation film and on and over an exposed part of the barrier film." In Hieda, no conductive film is ever formed on and over an exposed part of nitride film 21. For each of the aforesaid reasons, nitride film 21 in Hieda cannot be the claimed "barrier film" given the language

of claim 1. Given that claim 1 requires "making a contact hole in the barrier film and the interlayer insulating film *at the same time"* the only film in Hieda that could possibly be alleged to be the "barrier" is film 15.

However, assuming that film 15 in Hieda is a "barrier film", Hieda cannot possibly meet the aspect of claim 1 which requires "etching the insulation film until the barrier film is exposed, so as to leave the lower electrode in a protuberant manner." This is because Hieda's layer 15 is never exposed due to etching of an insulator in order to leave the lower electrode in a protuberant manner. Additionally, Hieda also fails to disclose or suggest "patterning the dielectric film and the second conductive film simultaneously to thereby form a capacitor dielectric film and an upper electrode" as required by claim 1 – in this respect, Hieda only mentions patterning of the plate electrode 27 (col. 12, lines 12-14, col. 16, lines 4-6).

In view of the above, it can be seen that Hieda cannot possibly anticipate or otherwise render unpatentable the invention of claim 1. Hieda is unrelated to the invention of amended claim 1 for the reasons discussed above.

New claims 10-11 state that the contact hole has the same cross sectional area in both the interlayer insulating film and the barrier film. For example, see Fig. 1 of the instant application which illustrates that hole 2a has the same cross sectional area in interlayer insulating film 2 and barrier film 3. Hieda fails to disclose or suggest a hole with the same cross sectional area in layers 14 and 21. Again, Hieda's layer 21 cannot be the claimed "barrier film."

Claim 12 requires that "the dielectric film covers each of an upper surface and all side surfaces of the protuberant lower electrode." For example, Fig. 1 of the instant application illustrates that dielectric film 9 (e.g., ferroelectric) covers both the upper surface of electrode 8 as well as the entire side surface(s) thereof. Hieda fails to disclose or suggest this aspect of claim 12.

Claim 4 also clearly defines over the cited art. Assuming that Hieda's layer 14 is an "interlayer insulator" as alleged in the Office Action, the nitride film 21 cannot possibly be the claimed "barrier film." This is because the holes in layers 14 and 21 are formed at very different points in time in Hieda (i.e., the hole in layer 21 is formed well after the hole in layer 14). See the discussion above in this respect.

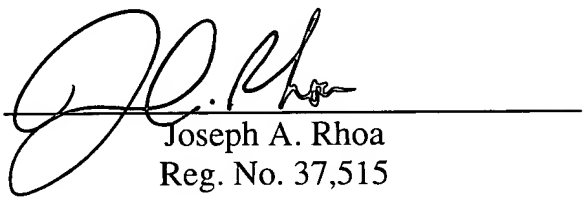
Still referring to claim 4, the claim requires "forming a second insulation film on the first conductive film so as to fill the hole; etching the second insulation film until an upper surface of the first conductive film is reached, and then etching the first conductive film and the second insulation film in the hole by a chemical mechanical polishing method until the first insulation film is exposed, to thereby form a cup-shaped lower electrode within the hole; etching the first insulation film and the second insulation film within the hole until the barrier film and the lower electrode are exposed; forming a dielectric film over the cup-shaped lower electrode such that the dielectric film covers inner and outer peripheries and an inner bottom surface of the cup-shaped lower electrode, and then forming a second conductive film that covers the dielectric film, said dielectric film being made of a ferroelectric or high-dielectric-constant substance; and patterning the dielectric film and the second conductive film simultaneously to thereby

form a capacitor dielectric film and an upper electrode." Hieda fails to disclose or suggest the aforesaid underlined aspects of claim 4. For example,

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please cancel claim 8, without prejudice in view of the Restriction Requirement.

1. (Amended) A method of producing a semiconductor device, the method comprising:

sequentially forming an interlayer insulating film and a barrier film on a semiconductor substrate;

making a contact hole in the barrier film and the interlayer insulating film at the same time and forming a plug within the contact hole;

forming an insulation film on the plug and the barrier film and then forming a hole in the insulation film leading to the plug [in the insulation film] such that an upper surface of the plug and part of the barrier film are [is] exposed;

forming a first conductive film on the insulation film and on and over an exposed part of the barrier film in the hole such that the hole in the insulation film is filled with the first conductive film, and then etching the first conductive film by a chemical mechanical polishing method to thereby form a lower electrode within the hole in the insulation film;

etching the insulation film until the barrier film is exposed, so as to leave the lower electrode in a protuberant manner;

forming a dielectric film that covers the protuberant lower electrode and at least part of the barrier film, and then forming a second conductive film that covers at least part of the dielectric film, said dielectric film being made of a ferroelectric or high-dielectric-constant substance; and

patterning the dielectric film and the second conductive film simultaneously to thereby form a capacitor dielectric film and an upper electrode.

4. (Amended) A method of producing a semiconductor device, the method comprising:

sequentially forming an interlayer insulating film and a barrier film [on] so as to be supported by a semiconductor substrate;

making a contact hole in the barrier film and the interlayer insulating film at the same time and forming a plug within the contact hole;

forming a first insulation film on the plug and the barrier film and then forming a hole leading to the plug in the first insulation film such that an upper surface of the plug is exposed;

forming a first conductive film over at least part of the first insulation film and within the hole such that the first conductive film within the hole does not fill the hole but covers surfaces defining the hole, and then forming a second insulation film on the first conductive film so as to fill the hole;

etching the second insulation film until an upper surface of the first conductive film is reached, and then etching the first conductive film and the second insulation film

in the hole by a chemical mechanical polishing method until the first insulation film is exposed, to thereby form a cup-shaped lower electrode within the hole;

etching the first insulation film and the second insulation film within the hole until the barrier film and the lower electrode are exposed;

forming a dielectric film over the cup-shaped lower electrode such that the dielectric film covers inner and outer peripheries and an inner bottom surface of the cup-shaped lower electrode, and then forming a second conductive film that covers the dielectric film, said dielectric film being made of a ferroelectric or high-dielectric-constant substance; and

patterning the dielectric film and the second conductive film simultaneously to thereby form a capacitor dielectric film and an upper electrode.

Please add the following new claims:

10. (New) The method of claim 1, wherein the contact hole has the same cross sectional area in both the interlayer insulating film and the barrier film.

11. (New) The method of claim 4, wherein the contact hole has the same cross sectional area in both the barrier film and the interlayer insulating film.

12. (New) The method of claim 1, wherein the dielectric film covers each of an upper surface and all side surfaces of the protuberant lower electrode.